ADC-XMC-STANDALONE
User Manual

Document Revision: 2.3
04/12/2024

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1 Introduction

The ADC-XMC-STANDALONE is a standalone carrier for Alpha-Data XMCs. The board provides Ethernet, Serial COM, USB, SATA, M.2 PCIe, QSFP, FireFly, GPIO and DisplayPort IO options. To allow compatibility with various XMC board pinouts, a personality wiring card that matches the XMC pinout is used to route signals through to the IO interfaces.

Apart from the IO functionality, the ADC-XMC-STANDALONE uses a single 15V-24V input power supply, and generates all supplies required by the XMC site internally. An on-board system monitor micro-controller provides voltage/current monitoring of the generated power supplies, as well as providing the capability to turn the supplies on/off via the micro USB interface. A USB to JTAG circuit is also provided, giving access to the JTAG chain without requiring an external JTAG box. Additionally, an on-board USB to UART converter circuit is also provided, removing the need for a dedicated USB to Serial cable.

IO interface support is dependent on the XMC type fitted, as well as the configuration of that XMC board.

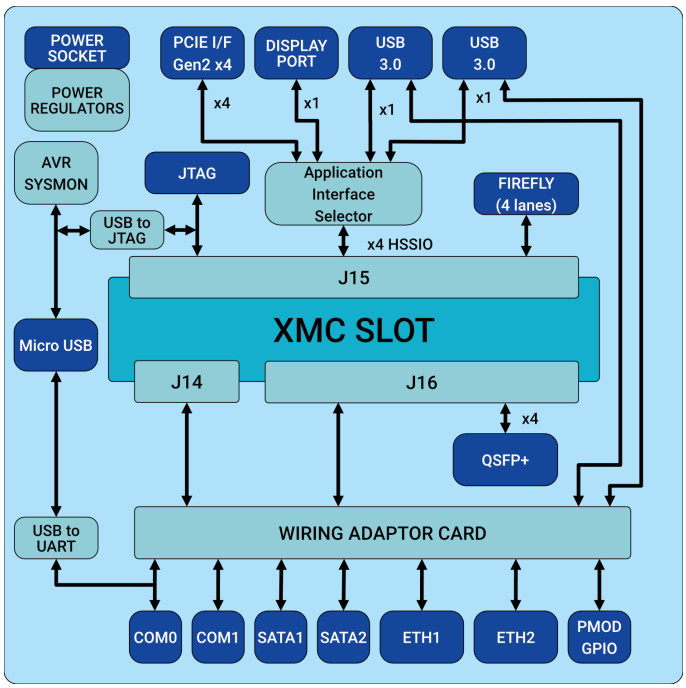

Figure 1 : ADC-XMC-STANDALONE Block Diagram

2 Board Features

The following photos highlight the various features of the ADC-XMC-STANDALONE

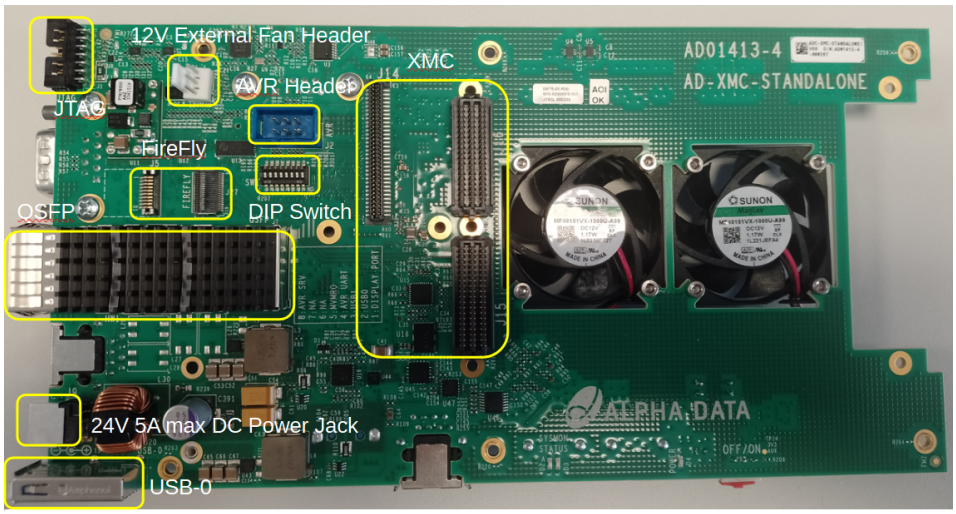

Figure 2 : ADC-XMC-STANDALONE Features

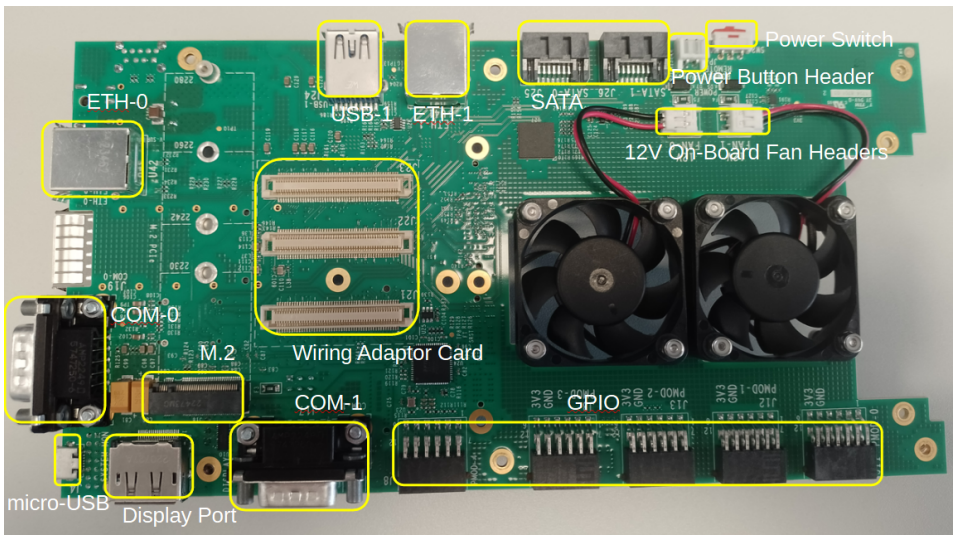

Figure 3 : ADC-XMC-STANDALONE Features

3 Switch Definitions

Default switch definitions are all OFF.

Switch	Description
SW1-1	DisplayPort Enable. Uses upper 2 PCIe lanes, limiting NVME devices to PCIe x2.
SW1-2	USB3 enable on USB-0 port J20. Uses PCIe lane 0, therefore effectively disabling NVME PCIe.
SW1-3	USB3 enable on USB-1 port J24. Uses PCIe lane 1, limiting NVME devices to PCIe x1.
SW1-4	Enables UART connection between system monitor and PMOD J3 pins 7, 8 and 9 (pins 1, 2 and 3 for rev 2 boards).
SW1-5	AVR service mode.
SW1-6	XMC MVMRO Enable.
SW1-7	Unused.
SW1-8	Unused.

Table 1 : Switch Definitions

4 M.2 Drive Selection

The ADC-XMC-STANDALONE has some components underneath the M.2 drive, so it's only recommended to be used with single-sided M.2 NVMe drives. Care must be taken to make sure there are no short-circuits if a double sided NVMe drive that requires a heatsink on the bottom is used.

5 Main Input Power Supply Requirements

The total power requirement for the main input supply will vary depending on the XMC board fitted, as well as the particular FPGA design within that board. A 60W supply would likely be more than enough for most FPGA designs before thermal limits of the device and heatsink become the limiting factor. Alpha-Data can provide a power supply estimator spreadsheet to estimate the total power requirements for a particular FPGA design with a particular XMC board.

Spec	Value
Voltage	15V-24V
Power	60W
Current	5A Max.
Connector	2.1mm x 5.5mm DC power plug, centre pin positive

Table 2 : Suggested Input Supply Specifications

6 Installation and Power Up

The required personality card should be attached to connectors J21, J22 and J23 on the rear of the board prior to attaching the XMC card to J14, J15 and J16.

To power up the board, ensure that power switch SW2 is OFF, and connect a 15V-24V power supply. To turn the board ON, switch the power switch SW2 to ON.

7 JTAG Interface

A USB to JTAG circuit is provided, giving access to the XMC JTAG interface without the need for an external programming box (e.g. Xilinx Platform Cable II). The USB to JTAG converter is compatibile with Vivado, and will appear in hardware manager as a Digilent device. A 14-pin JTAG header is also available, with an on-board multiplexer to switch between the 14-pin header or the USB to JTAG converter. The multiplexer selects the USB to JTAG circuit when a micro USB cable is attached.

8 USB to UART Interface

An on-board USB to UART circuit is provided, which allows the access to a serial terminal without the need to use a dedicated USB to Serial converter plus a serial cable. A multiplexer automatically selects between the USB J4 and the COM-0 J19 connectors to determine which transmits the serial data. J19 always has the priority and transmission data through J4 will be disabled if J19 is active. Receiving data is always active for both ports.

9 GPIO Interface

The GPIO is provided as a set of connectors conforming to the Digilent PMOD specification: https://digilent.com/reference/_media/reference/pmod/pmod-interface-specification-1_2_0.pdf

The PMOD connectors are 12-pin connectors, with two 3.3V VCC pins, two GND pins and 8 data pins:

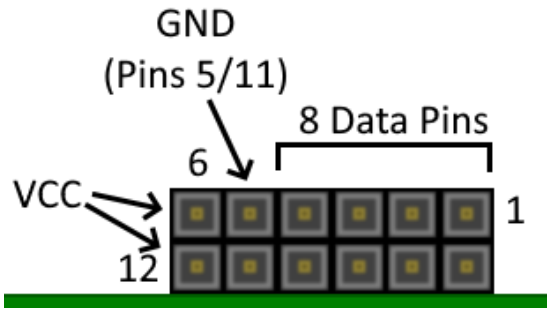

Figure 4 : PMOD Pinout

Maximum current draw on the VCC pins is not specified by the Digilent PMOD specification, but it recommends no more than approximately 100mA. On the ADC-XMC-STANDALONE, the 3.3V PMOD pins are connected directly to the main 3.3V power rail. This rail has a maximum current draw of 9.5A, although it is shared with the XMC board and other on-board devices, so total current draw of all PMOD devices should leave enough headroom for other devices on the 3.3V rail to operate.

There are a total of 5 PMOD connectors (J8, J3, J11, J12 and J13). The data pins of these connectors connect directly to the XMC J16 user defined IO pins. The GPIO pins connected to connector J8 also connect to the FireFly and QSFP sideband signals (I2C/RESET_L/INT_L/MODPRS_L), so are dual use. The FPGA pins that the PMOD data pins connect to are listed in section: Connector Pin Assignments when used with an XMC card. Some PMOD GPIO pins may be unconnected, depending on the number of GPIO pins available on the XMC card.

10 Current/Voltage Monitoring

The ADC-XMC-STANDALONE provides high-side current sense functionality on both the 12V and 3V3+3V3_AUX supplies. These values can be reported over the microUSB interface, using the alpha-data "avr2util" utility.

Avr2util for Windows and the associated USB driver can be downloaded here:
https://support.alpha-data.com/pub/firmware/utilities/windows/

Avr2util for Linux can be downloaded here:
https://support.alpha-data.com/pub/firmware/utilities/linux/

Use "avr2util.exe /?" to see all options.
For example "avr2util.exe /usbcom com4 display-sensors" will display all sensor values.

Note that 'com4' is used here as an example, and should be changed to match the com port number assigned under windows device manager

11 On-Board Generated Power Supplies

The ADC-XMC-STANDALONE generates the 3V3/3V3_AUX/12V0/-12V0 supplies required by the XMC site from a single 15V-24V input supply. Each supply has the following specifications:

Power supply	Voltage (V)	Max. current (A)	Monitoring
3V3_DIG	3.3	9.5 [1]	Voltage and current [1]
3V3_AUX	3.3 [2]	9.5 [1]	Voltage and current [1]
12V0_DIG	12.0	5	Voltage and current
-12V0_DIG	-12.0	1.5	Unmonitored

Table 3 : ADC-XMC-STANDALONE Power Supplies

[1] The 3V3_DIG and 3V3_AUX rails are generated from the same supply, so the maximum current is the combination of 3V3_AUX + 3V3_DIG. The current monitoring also measures the combined current.

[2] The 3V3_AUX rail is an always-on 3.3V auxiliary power supply from the 15V-30V input.

12 Connector Pin Assignments when used with an XMC card

The pinout depends on the personality board used. Select the correct table below for the pinout. **Any pins not listed in the tables below are NC.**

For ADC-XMC-STANDALONE REV 2 PCBs, the PMOD connector silkscreen has pins 1-7 swapped with pins 8-12. The pinout in the table below is correct as per the PMOD spec, but does not match the silkscreen.

Dual use pins (e.g. GPIO4/FIREFLY_SDA) are also routed to the QSFP/FireFly module's sideband control signals, as well as the GPIO headers. The I2C signals (SDA/SCL) have 4k32 on-board pull-ups to 3.3V, and the RESET_L/MODPRS_L/INT_L signals have 12k0 pull-ups to 3.3V

12.1 ADM-XRC-9R1/ADM-XRC-9R1-B pcb revision 3+ pinout

Connector Pin	J16 Pin	ADM-XRC-9R1/ ADM-XRC-9R1-B FPGA Pin	Function	Voltage Standard
J7.36	A1	B28	QSFP0 Tx+ (MGT129 3)	LVDS
J7.37	B1	B29	QSFP0 Tx- (MGT129 3)	LVDS
J7.17	A11	A31	QSFP0 Rx+ (MGT129 3)	LVDS
J7.18	B11	A32	QSFP0 Rx- (MGT129 3)	LVDS
J7.3	D1	C30	QSFP1 Tx+ (MGT129 2)	LVDS
J7.2	E1	C31	QSFP1 Tx- (MGT129 2)	LVDS
J7.22	D11	B33	QSFP1 Rx+ (MGT129 2)	LVDS
J7.21	E11	B34	QSFP1 Rx- (MGT129 2)	LVDS
J7.33	A3	D28	QSFP2 Tx+ (MGT129 1)	LVDS
J7.34	B3	D29	QSFP2 Tx- (MGT129 1)	LVDS
J7.14	A13	D33	QSFP2 Rx+ (MGT129 1)	LVDS
J7.15	B13	D34	QSFP2 Rx- (MGT129 1)	LVDS
J7.6	D3	E30	QSFP3 Tx+ (MGT129 0)	LVDS
J7.5	E3	E31	QSFP3 Tx- (MGT129 0)	LVDS
J7.25	D13	F33	QSFP3 Rx+ (MGT129 0)	LVDS
J7.24	E13	F34	QSFP3 Rx- (MGT129 0)	LVDS
J25.2	A5	G30	SATA0 Tx+ (MGT128 3)	LVDS
J25.3	B5	G31	SATA0 Tx- (MGT128 3)	LVDS
J25.6	A15	H33	SATA0 Rx+ (MGT128 3)	LVDS
J25.5	B15	H34	SATA0 Rx- (MGT128 3)	LVDS
J26.2	D5	J30	SATA1 Tx+ (MGT128 2)	LVDS
J26.3	E5	J31	SATA1 Tx- (MGT128 2)	LVDS

Table 4 : ADM-XRC-9R1/ADM-XRC-9R1-B PCB revision 3+ pinout for J16 (continued on next page)

Connector Pin	J16 Pin	ADM-XRC-9R1/ ADM-XRC-9R1-B FPGA Pin	Function	Voltage Standard
J26.6	D15	K33	SATA1 Rx+ (MGT128 2)	LVDS
J26.5	E15	K34	SATA1 Rx- (MGT128 2)	LVDS
J11.3	C7	D9	GPIO19	3.3V CMOS
J11.2	C8	C9	GPIO18	3.3V CMOS
J11.1	C9	B10	GPIO17	3.3V CMOS
J11.9	B19	F28	MGTREFCLK1P_129/GPIO_23	3.3V CMOS
J11.8	A19	F29	MGTREFCLK1N_129/GPIO_22	3.3V CMOS
J3.4	F14	C14	GPIO12	3.3V CMOS
J3.3	C14	C11	GPIO11	3.3V CMOS
J3.2	F15	K12	GPIO10	3.3V CMOS
J3.1	C15	E10	GPIO9	3.3V CMOS
J3.10	C10	B11	GPIO16	3.3V CMOS
J3.9	C11	A9	GPIO15	3.3V CMOS
J3.8	C12	E11	GPIO14	3.3V CMOS
J3.7	C13	D11	GPIO13	3.3V CMOS
J8.4	F18	A10	GPIO4/FIREFLY_SDA	3.3V CMOS
J8.3	C18	K10	GPIO3/QSFP_MODPRS_L	3.3V CMOS
J8.2	F19	C13	GPIO2/QSFP_SDA	3.3V CMOS
J8.1	C19	B13	GPIO1/QSFP_SCL	3.3V CMOS
J8.10	F16	E9	GPIO8/OPTICAL_INT_L	3.3V CMOS
J8.9	C16	H10	GPIO7/OPTICAL_RESET_L	3.3V CMOS
J8.8	F17	C10	GPIO6/FIREFLY_MODPRS_L	3.3V CMOS
J8.7	C17	H9	GPIO5/FIREFLY_SCL	3.3V CMOS

Table 4 : ADM-XRC-9R1/ADM-XRC-9R1-B PCB revision 3+ pinout for J16

Connector Pin	J14 Pin	Function	Voltage Standard
U41.1	1	Ethernet1 MD0+	1000-baseT
U41.2	3	Ethernet1 MD0-	1000-baseT
U41.3	7	Ethernet1 MD1+	1000-baseT
U41.6	9	Ethernet1 MD1-	1000-baseT
U41.4	2	Ethernet1 MD2+	1000-baseT
U41.5	4	Ethernet1 MD2-	1000-baseT
U41.7	8	Ethernet1 MD3+	1000-baseT
U41.8	10	Ethernet1 MD3-	1000-baseT
U42.1	13	Ethernet0 MD0+	1000-baseT
U42.2	15	Ethernet0 MD0-	1000-baseT
U42.3	19	Ethernet0 MD1+	1000-baseT
U42.6	21	Ethernet0 MD1-	1000-baseT
U42.4	14	Ethernet0 MD2+	1000-baseT
U42.5	16	Ethernet0 MD2-	1000-baseT
U42.7	20	Ethernet0 MD3+	1000-baseT
U42.8	22	Ethernet0 MD3-	1000-baseT
J19.3	43	COM1 Tx	RS232
J19.2	42	COM1 Rx	RS232
J17.3	47	COM2 Tx	RS232
J17.2	48	COM2 Rx	RS232
J24.3	27	USB1 Data+	USB
J24.2	25	USB1 Data-	USB
J24.1	29	USB1 Vcc	5V0 Power
J20.3	28	USB0 Data+	USB
J20.2	26	USB0 Data-	USB
J20.1	30	USB0 Vcc	5V0 Power

Table 5 : ADM-XRC-9R1/ADM-XRC-9R1-B pcb revision 3+ pinout for J14

12.2 ADM-XRC-9Z1 pcb pinout

Connector Pin	J16 Pin	ADM-XRC-9Z1 FPGA Pin	Function	Voltage Standard
J7.36	A1	T6	QSFP0 Tx+ (MGT228 0)	LVDS
J7.37	B1	T5	QSFP0 Tx- (MGT228 0)	LVDS
J7.17	A11	T2	QSFP0 Rx+ (MGT228 0)	LVDS
J7.18	B11	T1	QSFP0 Rx- (MGT228 0)	LVDS
J7.3	D1	R8	QSFP1 Tx+ (MGT228 1)	LVDS

Table 6 : ADM-XRC-9Z1 PCB pinout for J16 (continued on next page)

Connector Pin	J16 Pin	ADM-XRC-9Z1 FPGA Pin	Function	Voltage Standard
J7.2	E1	R7	QSFP1 Tx- (MGT228 1)	LVDS
J7.22	D11	R4	QSFP1 Rx+ (MGT228 1)	LVDS
J7.21	E11	R3	QSFP1 Rx- (MGT228 1)	LVDS
J7.33	A3	P6	QSFP2 Tx+ (MGT228 2)	LVDS
J7.34	B3	P5	QSFP2 Tx- (MGT228 2)	LVDS
J7.14	A13	P2	QSFP2 Rx+ (MGT228 2)	LVDS
J7.15	B13	P1	QSFP2 Rx- (MGT228 2)	LVDS
J7.6	D3	N8	QSFP3 Tx+ (MGT228 3)	LVDS
J7.5	E3	N7	QSFP3 Tx- (MGT228 3)	LVDS
J7.25	D13	N4	QSFP3 Rx+ (MGT228 3)	LVDS
J7.24	E13	N3	QSFP3 Rx- (MGT228 3)	LVDS
J8.1/J7.11	C19	K13	GPIO1/QSFP_SCL	3.3V CMOS
J8.2/J7.12	F19	H13	GPIO2/QSFP_SDA	3.3V CMOS
J8.3/J7.27	C18	L13	GPIO3/QSFP_MODPRS	3.3V CMOS
J8.4/J5.7	F18	J12	GPIO4/FIREFLY_SDA	3.3V CMOS
J8.7/J5.8	C17	L12	GPIO5/FIREFLY_SCL	3.3V CMOS
J8.8/J5.3	F17	G13	GPIO6/FIREFLY_MODPRS	3.3V CMOS
J8.9/J5.6/J7.9	C16	K12	GPIO7/OPTICAL_RESET	3.3V CMOS
J8.10/J5.5/J7.28	F16	H14	GPIO8/OPTICAL_INT	3.3V CMOS
J3.1	C15	J10	GPIO9	3.3V CMOS
J3.2	F15	J14	GPIO10	3.3V CMOS
J3.3	C14	G11	GPIO11	3.3V CMOS
J3.4	F14	K14	GPIO12	3.3V CMOS
J3.7	C13	H11	GPIO13	3.3V CMOS
J3.8	F13	J11	GPIO14	3.3V CMOS
J3.9	C12	G10	GPIO15	3.3V CMOS
J3.10	F12	K10	GPIO16	3.3V CMOS
J11.1	C11	F11	GPIO17	3.3V CMOS
J11.2	F11	H12	GPIO18	3.3V CMOS
J11.3	C10	F13	GPIO19	3.3V CMOS
J11.4	F10	F10	GPIO20	3.3V CMOS
J11.7	C9	E13	GPIO21	3.3V CMOS
J11.8	F9	E12	GPIO22	3.3V CMOS
J11.9	C8	D11	GPIO23	3.3V CMOS
J11.10	F8	F12	GPIO24	3.3V CMOS
J12.1	C7	E14	GPIO25	3.3V CMOS

Table 6 : ADM-XRC-9Z1 PCB pinout for J16 (continued on next page)

Connector Pin	J16 Pin	ADM-XRC-9Z1 FPGA Pin	Function	Voltage Standard
J12.2	F7	E10	GPIO26	3.3V CMOS
J12.3	C6	B13	GPIO27	3.3V CMOS
J12.4	F6	D14	GPIO28	3.3V CMOS
J12.7	C5	A13	GPIO29	3.3V CMOS
J12.8	F5	C13	GPIO30	3.3V CMOS
J12.9	C4	B14	GPIO31	3.3V CMOS
J12.10	F4	C14	GPIO32	3.3V CMOS
J13.1	C3	F15	GPIO33	3.3V CMOS
J13.2	F3	A15	GPIO34	3.3V CMOS
J13.3	C2	E15	GPIO35	3.3V CMOS
J13.4	F2	B15	GPIO36	3.3V CMOS
J13.7	C1	D15	GPIO37	3.3V CMOS
J13.8	F1	G14	GPIO38	3.3V CMOS
J25.2	A5	M6	SATA0 Tx+ (MGT229 0)	LVDS
J25.3	B5	M5	SATA0 Tx- (MGT229 0)	LVDS
J25.6	A15	M2	SATA0 Rx+ (MGT229 0)	LVDS
J25.5	B15	M1	SATA0 Rx- (MGT229 0)	LVDS
J26.2	D5	L8	SATA1 Tx+ (MGT229 1)	LVDS
J26.3	E5	L7	SATA1 Tx- (MGT229 1)	LVDS
J26.6	D15	L4	SATA1 Rx+ (MGT229 1)	LVDS
J26.5	E15	L3	SATA1 Rx- (MGT229 1)	LVDS
J16D.D17	D7	J8	DP+ (MGT229 3)	LVDS
J16E.E17	E7	J7	DP- (MGT229 3)	LVDS
J16D.D7	D17	J4	DP+ (MGT229 3)	LVDS
J16E.E7	E17	J3	DP- (MGT229 3)	LVDS
J16A.A17	A7	K6	DP+ (MGT229 2)	LVDS
J16B.B17	B7	K5	DP- (MGT229 2)	LVDS
J16A.A7	A17	K2	DP+ (MGT229 2)	LVDS
J16B.B7	B17	K1	DP- (MGT229 2)	LVDS
J16D.D19	D9	G4/U39	DP+ (MGT230 1/MGT505 3)	LVDS
J16E.E19	E9	G7/U35	DP- (MGT230 1/MGT505 3)	LVDS
J16D.D9	D19	G4/U38	DP+ (MGT230 1/MGT505 3)	LVDS
J16E.E9	E19	G3/U39	DP- (MGT230 1/MGT505 3)	LVDS
J16A.A19	A9	H6/W34	DP+ (MGT230 0/MGT505 2)	LVDS
J16B.B19	B9	H5/W35	DP- (MGT230 0/MGT505 2)	LVDS
J16A.A9	A19	V10	MGTREFCLK1P_228	LVDS

Table 6 : ADM-XRC-9Z1 PCB pinout for J16 (continued on next page)

Connector Pin	J16 Pin	ADM-XRC-9Z1 FPGA Pin	Function	Voltage Standard
J16B.B9	B19	V9	MGTREFCLK1N_228	LVDS

Table 6 : ADM-XRC-9Z1 PCB pinout for J16

Connector Pin	J14 Pin	Function	Voltage Standard
U41.1	1	Ethernet1 MD0+	1000-baseT
U41.2	3	Ethernet1 MD0-	1000-baseT
U41.3	7	Ethernet1 MD1+	1000-baseT
U41.6	9	Ethernet1 MD1-	1000-baseT
U41.4	2	Ethernet1 MD2+	1000-baseT
U41.5	4	Ethernet1 MD2-	1000-baseT
U41.7	8	Ethernet1 MD3+	1000-baseT
U41.8	10	Ethernet1 MD3-	1000-baseT
U42.1	13	Ethernet0 MD0+	1000-baseT
U42.2	15	Ethernet0 MD0-	1000-baseT
U42.3	19	Ethernet0 MD1+	1000-baseT
U42.6	21	Ethernet0 MD1-	1000-baseT
U42.4	14	Ethernet0 MD2+	1000-baseT
U42.5	16	Ethernet0 MD2-	1000-baseT
U42.7	20	Ethernet0 MD3+	1000-baseT
U42.8	22	Ethernet0 MD3-	1000-baseT
J19.3	43	COM1 Tx	RS232
J19.2	42	COM1 Rx	RS232
J17.3	47	COM2 Tx	RS232
J17.2	48	COM2 Rx	RS232
J24.3	27	USB1 Data+	USB
J24.2	25	USB1 Data-	USB
J24.1	29	USB1 Vcc	5V0 Power
J20.3	28	USB0 Data+	USB
J20.2	26	USB0 Data-	USB
J20.1	30	USB0 Vcc	5V0 Power
J13.10	51	CANH	CAN
J13.9	53	CANL	CAN

Table 7 : ADM-XRC-9Z1 pcb pinout for J14

13 Dimensions

Dimension	Measurement
X PCB	219mm
X including connectors	225.55mm
Y PCB	112.5mm
Y including connectors	114.95mm
Z PCB	1.63mm
Z including connectors	30.36mm

Table 8 : ADC-XMC-STANDALONE PCB dimensions

14 Order Code

ADC-XMC-STANDALONE/X/T

Name	Symbol	Configurations
XMC Personality Card	x	9R1 = ADM-XRC-9R1/ADM-XRC-9R1-B, 9Z1 = ADM-XRC-9Z1
XMC Connector Type	t	blank = XMC (VITA 42) Connectors, /V88 = XMC+ (VITA 88) Connectors

Table 9 : ADC-XMC-STANDALONE Order Code

Revision History

Date	Revision	Nature of Change
22 Feb 2021	1.0	Preliminary issue
18 May 2021	1.1	Added board diagram, added PMOD connector pin numbers, added 9R1 FPGA pin numbers
14 Oct 2021	1.2	Added description of the USB to JTAG, moved pin assignments to the end of the document
21 July 2022	1.4	Added P6 MGT refclk to 9R1 IO tables
05 October 2022	1.5	Added M.2 drive selection section
31 October 2022	1.6	Clarified PMOD due to pins 1-6 being swapped with 7-12
2 December 2022	1.7	Added switch defintions
4 January 2023	1.8	Added section describing GPIO PMOD connectors
15 November 2023	1.9	Fixing incorrect PMOD pin numbers in description for SW1-4
15 January 2024	2.0	Updating GPIO_22/GPIO_23 signal name to more accurately reflect the pin usage on the 9R1.
12 March 2024	2.1	Updated MGT bank numbers for QSFP/SATA when used with the 9R1.
09 September 2024	2.2	Fixed typos, block diagram updated, added updated top and bottom features pictures, switch definitions PMOD clarification between revisions, added USB to UART section, added connector pins to pinout tables, added 9Z1 pinout tables
04 December 2024	2.3	Added ADM-XRC-9R1-B to 9R1 tables

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